circuit 40 of Fig. 6 in that a command input buffer/latch circuit 244 is provided instead of command input buffer/latch circuit 44, and a delay circuit 251 is included. The remaining structure is similar to that of command generation circuit 40, and description thereof will not be repeated.

Delay circuit 251 includes a one cycle delay circuit 254 delaying the input signal for a delay time corresponding to one cycle of the refresh cycle to output a row active delay signal ACTD, and a latch circuit 252 set by row active command signal ACT and reset by row active delay signal ACTD to output a delay period display signal ACT_ACTD.

Command input buffer/latch circuit 244 differs in that a row active command signal ACT0 is transmitted to the internal command generation circuit irrespective of the state of refresh activation signal REF_RAS .

Row selection control circuit 241 differs from row selection control circuit 41 in that a refresh control circuit 250 is provided instead of refresh control circuit 50 in the structure of row selection control circuit 41 of Fig. 6. The remaining structure is similar to that of row selection control circuit 41, and description thereof will not be repeated.

Fig. 17 is a circuit diagram showing a structure of refresh control circuit 250 of Fig. 16.

Referring to Fig. 17, refresh control circuit 250 includes an inverter 262 receiving and inverting refresh activation signal REF_RAS , a latch circuit 264 set according to refresh request signal FAY and reset according to an output of inverter 262, an OR circuit 266 receiving an inverted output /Q of latch circuit 264, a delay time display signal ACT_ACTD and normal operation signal ACT_RAS, and a pulse generation circuit 268 receiving the output of OR circuit 266 to generate a pulse. Pulse generation circuit 268 outputs an internal refresh command signal REF.

Fig. 18 is a circuit diagram showing a structure of one cycle delay circuit 254 of Fig. 16.

Referring to Fig. 18, one cycle delay circuit 254 includes delay units 254#1-254#n connected in series to receive and delay for a predetermined time a row active command signal ACT. Delay unit 254#n outputs a row active delay signal ACTD.